**REMARKS**

In the Office Action mailed July 31, 2007 the Examiner noted that claims 1-4, 9-13, 15-18, 23-27, and 29-32 were pending and rejected claims 1-4, 9-13, 15-18, 23-27, and 29-32. Claims 1, 13, 15, 27, 29 and 30-32 have been amended, no claims have been canceled, new claim 33 has been added and, thus, in view of the forgoing, claims 1-4, 9-13, 15-18, 23-27, and 29-33 remain pending for reconsideration which is requested. No new matter has been added. The Examiner's rejections are traversed below.

REJECTION OF CLAIM 31 UNDER 35 U.S.C. § 112

Claim 31 stands rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Specifically, the Examiner cited indistinct language in the feature "two transfer to addresses for the data written." Claim 31 has been amended to recite correctly "two transferred-to addresses for the data written." This amendment properly recites the "transferred-to addresses," feature as that feature appears in other claims. Applicants submit that presently amended claim 31 is in condition for allowance. Favorable reconsideration and a withdrawal of the rejection is respectfully requested.

REJECTION OF CLAIM 32 UNDER 35 U.S.C. § 102

Claim 32 is rejected under 35 U.S.C. § 102(e) as anticipated by Avraham, U.S. Patent Pub. No. 2004/0103238. Avraham para. [0054], cited by the Examiner in the outstanding Office Action describes that data is written to nonvolatile memory when the cache is determined to be full or when there is a power interruption. *see* para. [0054], FIG. 3. The cache periodically may become full because system data is being cached onto the cache. para. [0054], lines 10-11. That is, when the cache is determined to be full, all mirroring of data from nonvolatile memory to volatile cache memory halts while the appliance moves all of the current volatile memory cache contents onto the nonvolatile memory. Once the cache has been copied over and cleared, then system data caching is then resumed.

In contrast, claim 32 is not directed towards a method that copies over the entire contents of the master area of a first memory module to a mirror area of a second memory module when it is determined that the master area of a first memory module is insufficient for a

data input request, rather, when the master area of a first memory module is determined to be insufficient for a data input request, the data "initially directed to the master area of a first memory module" (claim 32, line 5) is stored in the mirror area of a second memory module.

Moreover, Claim 32 has been amended to recite that the storing data initially directed to the master area is "from said data input request" to clarify this feature. In contrast, the data written in Avraham is not from a data input request, but rather the entire contents of a full cache memory module. Thus Appliants respectfully submit that Avraham does not teach or suggest the recited features of claim 32.

A withdrawal of the rejection and favorable reconsideration of claim 32 is respectfully requested.

REJECTION OF CLAIMS 1-4, 9-13,15-18, 23-27 and 29-30 UNDER 35 U.S.C. § 103

Claims 13, 27 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Weber, U.S. Patent No. 5,937,174 in view of Hauck, U.S. Patent Pub. No. 2003/0158999, in further view of Avraham.

PRIOR ART

Weber is directed to a cache memory control architecture within a RAID storage system. Hauck is a method of retaining cache coherency in a controller.

The Claims Patentably Distinguish Over the Prior Art

On page 5 of the Office Action, the Examiner cited to Fig. 2 and col. 7, line 47 – col. 8, lines 39 of Weber as describing the following feature of claim 13:

> a first module for controlling an interface to an external apparatus;
>
> a plurality of second modules each having a cache memory; and
>
> a bridge module connected through an interface bus to said first and second modules for accomplishing a connection between said first module and said second modules for data transfer there between,
>
> said first module writing data to be written, which is received from said external apparatus, through said bridge module into said cache memories of two of said plurality of second modules,

Applicants respectfully submit that nowhere in Weber is taught or described "a bridge module connected through an interface bus to said first and second modules" – the second modules each having a cache memory. First, Weber describes communication with a *disk storage system* and not cache. Second, the bus bridge 206 is connected to the high speed host

interface 204, and transfers data to a main memory controller 212, not to the device/disk interfaces 138.1. The bus bridge 206 of Weber communicates with the high speed host and main memory controller only. See col. 8, lines 27-32. Weber describes that it is the bus bridges 208 and 210 (bridges not connected to the high speed host interface 204) that provide the exchange of information between RAID array 104 and high speed cache buffer under the control of main memory controller 212. See col. 8, lines 32-39.

Moreover, claims 13 and 30 have been amended to recite "a bridge module connected ... to said first and second modules, without connecting through any other bridge modules." Also, Claim 27 has been amended also to recite "a bridge module connected ... to said disk interface module, without connecting through any other bridge modules." As Weber describes a bus bridge that connects to other modules only through other bridge modules, Weber does not teach or suggest the features of claims 13, 27 and 30.

Thus, none of Weber, Hauck or Avraham, whether considered alone, or in combination teach or suggest the elements of claim 13.

Claim 27 recites inter alia:

> a disk interface module for controlling an interface to said disk unit;
>
> a host interface module for controlling an interface to said host;
>
> a plurality of management modules for controlling the entire control apparatus; and
>
> a bridge module connected through an interface bus to said disk interface module, without connecting through any other bridge modules, said host interface module and said management modules for making connections among said disk interface module, said host interface module and said management modules for data transfer among said modules, the bridge module producing address information for two transferred-to addresses for the data written to the at least two management modules of the plurality of management modules,
>
> said host interface module writing data to be written, which is received from said host, through said bridge module into cache memories of two of said plurality of management modules

Therefore, it is submitted that claim 27 patentably distinguishes over the prior art.

Claim 30 recites inter alia:

> a first module controlling an interface to an external apparatus;
>
> a plurality of second modules each having a cache memory; and
>
> a bridge module connected through an interface bus to said first

> and second modules, without connecting through any other bridge modules, for accomplishing a connection between said first module and said second modules for data transfer there between, the bridge module producing address information for two transferred-to addresses for the data written to the at least two second modules of the plurality of second modules,
>
> said first module writing data to be written, which is received from said external apparatus, through said bridge module into said cache memories of two of said plurality of second modules

Therefore, it is submitted that claim 30 patentably distinguishes over the prior art.

On page 8, item 6 of the Office Action, claims 1-4, 9-12, 15-18, 23-26 and 29 were rejected under 35 U.S.C. § 103(a) as being obvious over the combined teachings of Weber, Hauck, Avraham and in further view of U.S. Patent Application Publication No. US 2002/0016898 by Hashimoto et al.

On page 9 of the outstanding office action, the Examiner cited to Weber at col. 8, lines 20-39 as describing the following feature of independent claims 1: "bridge module including: address production means ... to produce two transferred-to addresses for designation of said two second modules having cache memories... " (claim 1, lines 11-14). First, as mentioned above, the "bus bridge" in Weber that is connected to the high speed host interface is not connected to the device/disk interfaces.

Second, each of the bus bridges in Weber "adapts the signals applied to their respective, unique, connected bus architecture to the intermediate shared memory bus." See col. 8, lines 23-26. Thus, the purpose of these buses is to convert a signal from one bus to another, and nothing about addresses for designation of two second modules is taught or suggested here. Weber is directed towards the "porting of existing ("legacy") control methods and structures to newer high performance cache memory designs." See Abstract lines 2-4. Thus, "The bus bridge circuits each adapt, for example, a PCI bus used for a particular cache access purpose to the signal standards of an intermediate shared memory bus." See Abstract lines 8-11.

Moreover, independent claim 1 has been amended to recite "a bridge module connected ... without connecting through any other bridge modules." Thus Applicants submit that none of Weber, Hauck, Avraham and Hashimoto, whether considered alone or in combination teach or suggest the features of claim 1.

Claims 2-4 and 9-12 depend either directly or indirectly from claim 1 and include all the features of that claim plus additional features which are not taught or suggested by the prior art. Therefore, it is submitted that claims 2-4 and 9-12 patentably distinguish over the prior art.

Currently amended claim 15 recites inter alia:

> a host interface module for controlling an interface to said host;
>
> a plurality of management modules, each including a cache memory, for controlling the entire apparatus; and
>
> a bridge module connected through an interface bus to said disk interface module, without connecting through any other bridge modules, said host interface module and said management modules for making connections among said disk interface module, said host interface module and said management modules for data transfer among said disk interface module, said host interface module and said management modules,
>
> said host interface module including:
>
> address designation means for producing addressing information to designate two written-in destinations for writing data to be written, which is received from said host, through said bridge module into said cache memories of two of said plurality of management modules

Therefore, it is submitted that claim 15 patentably distinguishes over the prior art.

Claims 16-18 and 23-26 depend either directly or indirectly from claim 15 and include all the features of that claim plus additional features which are not taught or suggested by the prior art. Therefore, it is submitted that claims 16-18 and 23-26 patentably distinguish over the prior art.

Currently amended claim 29 recites inter alia:

> a plurality of second modules each having a cache memory; and
>
> a bridge module connected through an interface bus to said first and second modules, without connecting through any other bridge modules, for accomplishing a connection between said first module and said second modules for data transfer there between,
>
> said first module including an address designator producing addressing information to designate two written-in destinations for writing data to be written, which is received from said external apparatus, through said bridge module into said cache memories of two of said plurality of second modules

Therefore, it is submitted that claim 29 patentably distinguishes over the prior art.

NEW CLAIM 33

New claim 33 recites a storage control method which includes:

> transferring data to two cache modules using two transferred-to

addresses; and

storing data, from a data input request in a mirror area of one cache module, when a master area of the other cache module is insufficient for the data input request.

Therefore, it is submitted that claim 33 patentably distinguishes over the prior art.

SUMMARY

It is submitted that the claims continue to be allowable. It is further submitted that the claims are not taught, disclosed or suggested by the prior art. The claims are therefore in a condition suitable for allowance. An early Notice of Allowance is requested.

If any further fees, other than and except for the issue fee, are necessary with respect to this paper, the U.S.P.T.O. is requested to obtain the same from deposit account number 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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John C. Garvey
Registration No. 28,607

1201 New York Avenue, NW, 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1500